# Lab 3 Behavioral Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? Yes

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: Jiwon Youn

Student Name: Wonhee Lee  
Student ID: 54872959  
Date Completed: 05-14-2020  
Time Spent: Reviewing Digital Design Material: 1h  
 Design/Preparation Work: 1h  
 VHDL Coding & Debugging: 4h

## Behavioral Overview

100%

I feel confident with the result. Tested Rst = 1 to check whether it goes back to initial state, and it worked. Done also goes from 1 to 0 as it is reset. The result is 381 as expected. The calculation made few errors at first, but solved it through using multiple ‘temp’ variables.

## Lab 3 FSMD



## Lab 3 Behavioral Simulation Graph

